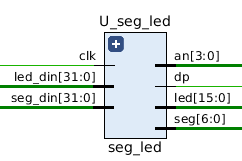
SEG-LED

# 1.1 implementation



Signal list:

in clk: clock signal

in led\_din: LED input

in seg\_din: SEG input

in reset: RESET for 7-seg

out an: SEG output

out dp: HIGH when running

out led: LED output

out seg: SEG output

This is a unit for showing the data by led and/or 7-seg.

# 1.2 Testbench

For this unit, we only need to set the input and check if it is working.

# 1.3 functional simulation

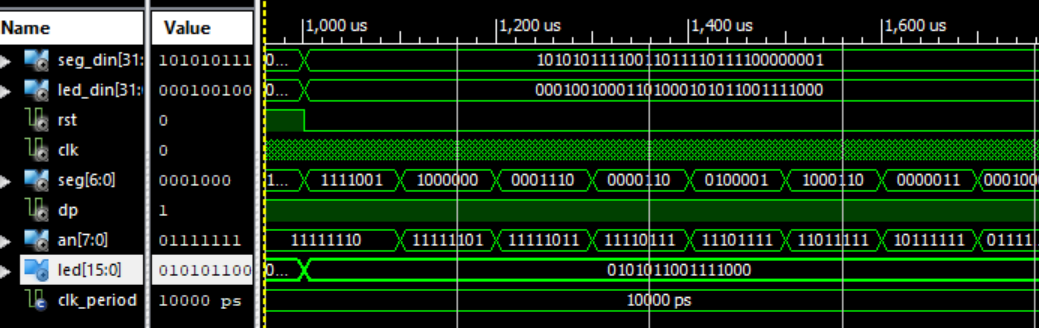


Figure 1.3.1 led and seg are working

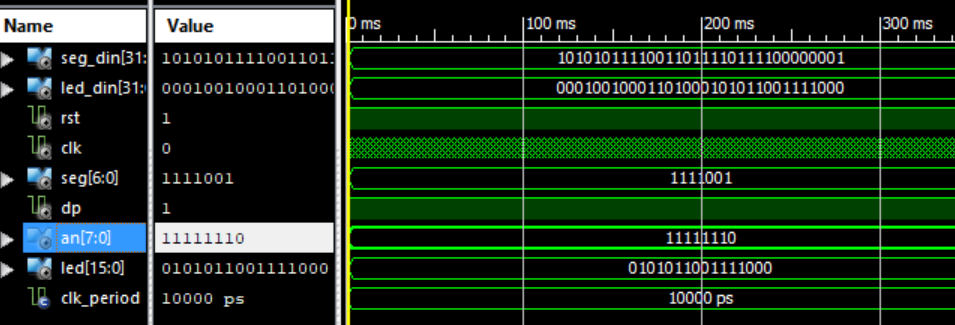


Figure 1.3.2 when reset is on, led working, seg stopped

# 1.4 timing simulation

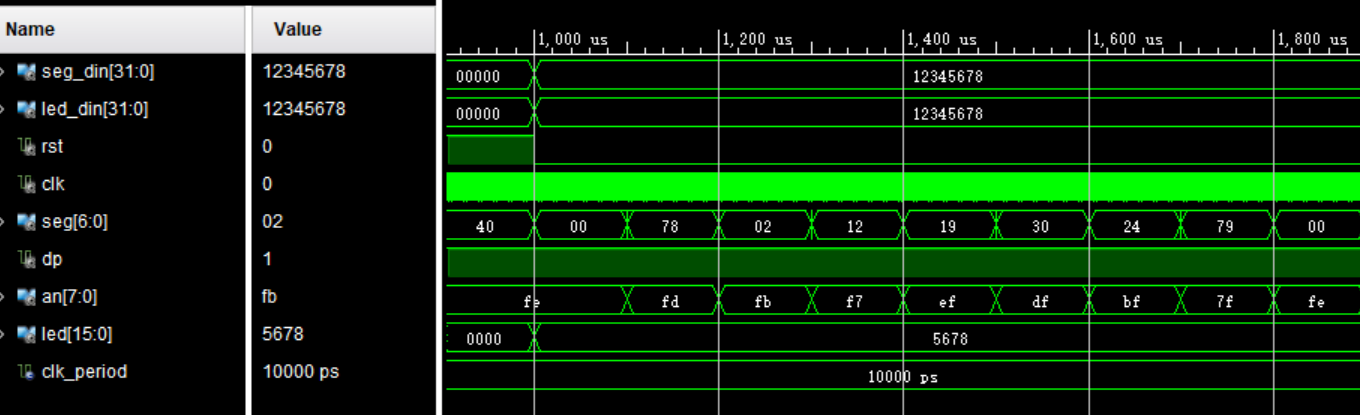


Figure 1.3.1 led and seg are working

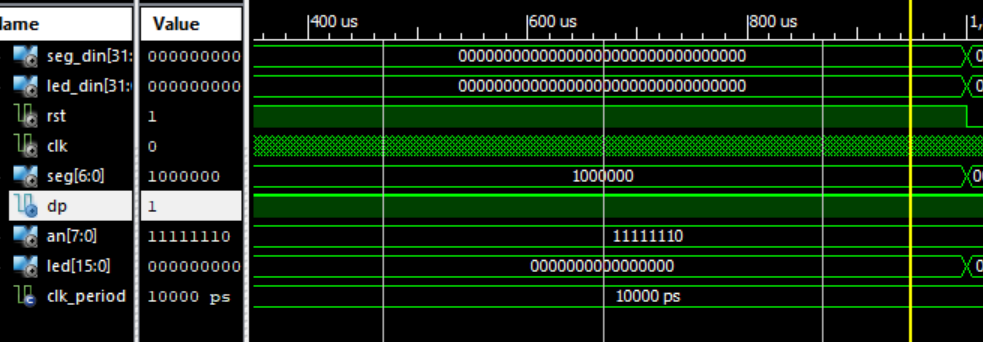


Figure 1.3.2 when reset is on, led working, seg stopped

# 1.5 Timing analysis

|  |  |
| --- | --- |
| Critical path delay | 6.0 ns |
| Highest frequency | 167 MHz |